	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	46958	silicon adj nitride	USPAT; US-PGPUB	2002/05/31 14:42
2	BRS	L2	873	1 with tantalum adj oxide	USPAT; US-PGPUB	2002/05/31 14:53
3	BRS	L3	4	2 and monos	USPAT; US-PGPUB	2002/05/31 14:54
4	BRS	L4	208	1 with (bst or (barium adj strontium))	USPAT; US-PGPUB	2002/05/31 14:54
5	BRS	L5	0	4 and monos	USPAT; US-PGPUB	2002/05/31 14:56
6	BRS	L6	1	4 and mnos	USPAT; US-PGPUB	2002/05/31 14:54
7	BRS	L7	0	4 same (charge adj storage)	USPAT; US-PGPUB	2002/05/31 14:57
8	BRS	L8	18	4 and (charge adj storage)	USPAT; US-PGPUB	2002/05/31 14:57

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BPS	L1	46958	silicon adj nitride	USPAT; US-PGPUB	2002/05/31 14:42
2	BRS	L2	873	1 with tantalum adj oxide	USPAT; US-PGPUB	2002/05/31 14:53
3	BPS	L3	4	2 and monos	USPAT; US-PGPUB	2002/05/31 14:54
4	BPS	L4	208	1 with (bst or (barium adj strontium))	USPAT; US-PGPUB	2002/05/31 14:54
5	BPS	L5	0	4 and monos	USPAT; US-PGPUB	2002/05/31 14:56
6	BPS	L6	1	4 and mnos	USPAT; US-PGPUB	2002/05/31 14:54
7	BPS	L7	0	4 same (charge adj storage)	USPAT; US-PGPUB	2002/05/31 14:57
8	BPS	L8	18	4 and (charge adj storage)	USPAT; US-PGPUB	2002/05/31 14:57

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 6449293 B1	20020514	36	Nonvolatile memory cell, operating method of the same and nonvolatile memory array	257/365	257/324; 257/411	Ogura, Seiki O. et al.
2	US 6255166 B1	20010703	21	Nonvolatile memory cell, method of programming the same and nonvolatile memory array	438/257	365/182; 365/185.27; 365/185.28; 365/185.29; 365/218; 365/53; 438/300; 438/350	Ogura, Seiki et al.
3	US 6281142 B1	20010828	16	Dielectric cure for reducing oxygen vacancies	438/771	257/103; 257/236; 257/240; 257/310; 322/10; 438/240; 438/402; 438/404	Basceri, Cem et al.
4	US 6201276 B1	20010313	16	Method of fabricating semiconductor devices utilizing in situ passivation of dielectric thin films	257/315		Agarwal, Vishnu K. et al.
5	US 6147011 A	20001114	10	Methods of forming dielectric layers and methods of forming capacitors	438/783	427/569; 427/574; 427/579; 438/778; 438/784; 438/785	Derderian, Garo J. et al.

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
.	[illegible] 5338954 A	[illegible]	14	Semiconductor memory device having an insulating film and a trap film joined in a channel region	257/326	257/316; 257/324	Shimoji, Noriyuki
2	[illegible] 6146904 A	[illegible]1114	10	Method of making a two transistor ferroelectric memory cell	438/3	438/240	Hsu, Sheng Teng et al.
3	[illegible] 6048738 A	[illegible]0411	13	Method of making ferroelectric memory cell for VLSI RAM array	438/3	438/240; 438/253	Hsu, Sheng Teng et al.
4	[illegible] 5999444 A	[illegible]1207	45	Nonvolatile semiconductor memory device and writing and erasing method of the same	365/185.02	365/185.18; 365/185.23	Fujiwara, Ichiro et al.
5	[illegible] 5737261 A	[illegible]0407	18	Non-volatile ferroelectric memory utilizing residual polarization of a ferroelectric film	365/145	257/295; 365/149	Taira, Shigenobu
6	U.S 5619051 A	[illegible]0409	11	Semiconductor nonvolatile memory cell	257/316	257/324; 257/325; 257/411	Endo, Nobuhiro